

A 10b 1MS/s 0.5mW SAR ADC with double sampling technique

Lee T., Kim M.-Y., Kim Y., Pham P.-H.

Dept. of Electrical Engineering, Korea University, Seoul, South Korea; Department of Electrical Engineering, Texas A and M University, TX, United States; Faculty of Electronics and Telecommunication, Vietnam National University, Hanoi, Viet Nam

Abstract: This paper introduces the 10b 1MS/s 0.5mW SAR ADC with double sampling technique. It utilizes the double sampling technique to reduce power. The SAR ADC is implemented in CMOS 1P8M 65nm technology and occupies $0.111\mu\text{m}^2$. The maximum sampling rate is 1MS/s. The simulated SNDR and SFDR are 55.6dB and 62.7dB, respectively at input frequency of 484kHz. Power consumption of the data converter is total 507uW with 1.2-V supply. ©2009 IEEE.

Author Keywords: 1MS/s, 10b, 1mW; ADC; Data converter; Double sampling; SAR

Index Keywords: 65nm technology; Data converter; Double sampling; Double sampling technique; Input frequency; Power Consumption; Sampling rates; SAR ADC; Programmable logic controllers; Multicarrier modulation

Year: 2009

Source title: 2009 International SoC Design Conference, ISOCC 2009

Art. No.: 5423831

Page : 512-515

Link: Scopus Link

Correspondence Address: Lee, T.; Dept. of Electrical Engineering, Korea University, Seoul, South Korea

Conference name: 2009 International SoC Design Conference, ISOCC 2009

Conference date: 22 November 2009 through 24 November 2009

Conference location: Busan

Conference code: 80004

ISBN: 9.78E+12

DOI: 10.1109/SOCCDC.2009.5423831

Language of Original Document: English

Abbreviated Source Title: 2009 International SoC Design Conference, ISOCC 2009

Document Type: Conference Paper

Source: Scopus

Authors with affiliations:

- Lee, T., Dept. of Electrical Engineering, Korea University, Seoul, South Korea
- Kim, M.-Y., Dept. of Electrical Engineering, Korea University, Seoul, South Korea
- Kim, Y., Department of Electrical Engineering, Texas A and M University, TX, United States
- Pham, P.-H., Faculty of Electronics and Telecommunication, Vietnam National University, Hanoi, Viet Nam

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