

# A low-power programmable DLL-based clock generator with wide-range anti-harmonic lock

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**Abstract:** A delay-locked loop (DLL)-based clock generator for dynamic frequency scaling has been developed in a 0.13 $\mu$ m CMOS technology. The proposed clock generator can generate a wide-range of the multiplied clock signals ranging from 125MHz to 2GHz. In addition, thanks to the proposed anti-harmonic lock block, the clock generator can change the frequency dynamically in one cycle time of the reference clock. The proposed DLL-based clock generator occupies 0.019mm<sup>2</sup> and consumes 21mW at 2GHz. The ratio of power consumption to frequency of the proposed clock generator is smaller than those of conventional ones. ©2009 IEEE.

**Author Keywords:** Anti-harmonic lock; Frequency multiplier

**Index Keywords:** Clock generator; Clock signal; CMOS technology; Cycle time; Delay-locked loops; Dynamic frequency scaling; Frequency multiplier; Low Power; Power Consumption; Reference clock; CMOS integrated circuits; Frequency multiplying circuits; Harmonic analysis; Programmable logic controllers; Electric clocks

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