Analysis and evaluation of traffic-performance in a backtracked routing network-on-chip

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Abstract: VLSI designers recently have adopted micro network-on-chip (or NoC) as an emerged solution to design complex SoC system under stringent constraints pertaining cost, size, power consumption, and short time-to-market. Characterization of on-chip traffics and traffic-performance evaluation are necessary steps bringing comprehensive and effective NoC design. This paper presents an analysis and performance evaluation framework of backtracked routing Network-on-Chip that provides guaranteed and energy-efficient data transfer. Experimental results, under common and application-oriented synthetic traffics, figure out the performance in terms of latency and throughput and suggest a tradeoff to developers to map applications into a proposed NoC platform. ©2008 IEEE.
Author Keywords: Network architecture; Network-on-chip; On-chip communication; On-chip traffics; Performance evaluation
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